ABSTRACT OF THE DISCLOSURE

A method and circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, such that the leading edges of the pulses occur at least nearly periodically, with time-averaged frequency at least nearly equal to $(A/T)F_i$, where A and T are integers, and such that the accumulated error, between the actual time interval between the first and last leading edges of Z consecutive ones of the pulses and the time $ZT/(AF_i)$, never exceeds $1/F_i$. When F_i is equal to $(T/A)F_o$, where F_o is a predetermined output line frequency, an embodiment of the sync pulse generator includes an accumulator which stores a Count value, a comparator, and logic circuitry for generating the sync pulse train in response to a binary signal asserted by the comparator (and typically also control data that determines a configuration of the logic circuitry). The Count value is set to zero in response to a Frame Start event, and then increases by the above-noted integer value, A, once per input clock cycle. During each input clock cycle, the comparator compares the Count value in the accumulator with the above-noted integer value, T. In response to the comparator output indicating that the Count value has risen to a value greater than or equal to T, the Count value in the accumulator is reduced by the value T – A and the logic circuitry asserts the leading edge of a sync pulse. In typical cases in which the sync pulses are for use in clocking, generating, or synchronizing with a video signal (and the initial value is zero), the ratio T/A is equal to the number of input clock cycles per line of the video signal (i.e., the number of input clock cycles required to clock out a line of the video signal to a display device using an output clock having the output clock frequency).